translating digital communications provided at said first apparatus connector in said first protocol into digital communications at said second apparatus connector in said second protocol through said first protocol processor and then said second protocol processor; and

translating digital communications provided at said second apparatus connector in said second protocol into digital communications at said first apparatus connector in said first protocol through said second protocol processor and then said first protocol processor.

16 36. (new) A method for plug-and-play compatibility as recited in claim 35, 15 wherein enabling said first protocol driver includes selecting said first protocol driver from a collection of drivers stored in a memory coupled to said first protocol processor.

17 37. (new) A method for plug-and-play compatibility as recited in claim 35, 15 wherein enabling said first protocol driver includes downloading said first protocol driver through said first apparatus connector to a memory coupled to said first protocol processor.

18 38. (new) A single chip protocol translator comprising:

a unitary semiconductor substrate integrating a translation circuitry; and

a memory coupled to said translation circuitry, wherein said translation circuitry is capable of communicating with first external devices with a first protocol and with second external devices with a second protocol, said first protocol being different from said second protocol, and wherein said first protocol is implemented with a first driver stored in said memory and said second protocol is implemented with a second driver stored in said memory.

19 39. (new) A single chip protocol translator recited in claim 38, 18 wherein said memory stores a collection of drivers, and wherein said translation circuitry selects an appropriate driver for at least one of said first driver and said second driver selected from said collection of drivers.

20 40. (new) A single chip protocol translator recited in claim 38, 18 wherein at least one of said first driver and said second driver is loaded into memory from at least one of said collection of drivers.

41. (new) A method for plug-and-play compatibility of a protocol translation circuitry, said method comprising:

determining a first communication protocol received at a first group of terminals of said protocol translation circuitry;

enabling a first protocol driver appropriate to said determined first protocol in a first protocol processor within said protocol translation circuitry;

translating digital communications in said first protocol provided at said first group of terminals into digital communications in a second protocol at a second group of terminals through said first protocol processor and then a second protocol processor; and

translating digital communications in said second protocol provided at said second group of terminals into digital communications in said first protocol at said first group of terminals through said second protocol processor and then said first protocol processor.

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42. (new) A method for plug-and-play compatibility as recited in claim 41, wherein enabling said first protocol driver includes selecting said first protocol driver from a collection of drivers stored in a memory coupled to said first protocol processor.

43. (new) A method for plug-and-play compatibility as recited in claim 41, wherein enabling said first protocol driver includes downloading said first protocol driver through said first group of terminals to a memory coupled to said first protocol processor.

44. (new) A protocol translation circuitry for plug-and-play compatibility, comprising:

a first group of terminals for receiving first digital communications in a first protocol;

a second group of terminals for receiving second digital communications in a second protocol;

a first protocol processor coupled to said first group of terminals; and

a second protocol processor coupled to said second group of terminals, wherein said first protocol processor determines said first protocol received at said first group of terminals and enables in said first protocol processor a first driver appropriate to said determined first protocol, and wherein said first digital communications provided at said first group of terminals in said first protocol are translated through said first protocol processor and then said second protocol processor into translated first digital communications in said second protocol at said second group of terminals, and said second digital communications received

at said second group of terminals in said second protocol are translated through said second protocol processor and then said first protocol processor into translated second digital communications in said first protocol at said first group of terminals.

45. (new) A protocol translation circuitry as recited in claim 44, further comprising a memory coupled to said first protocol processor, wherein said memory stores a collection of protocol drivers, and said first protocol processor selects said first protocol driver from said collection of protocol drivers.

46. (new) A protocol translation circuitry as recited in claim 44, further comprising a memory coupled to said first protocol processor, wherein said first protocol driver is loaded through said first group of terminals into said memory.

47. (new) A cable assembly for plug-and-play capability between a first apparatus capable of digitally communicating with a first protocol through a first apparatus connector and a second apparatus capable of digitally communicating with a second protocol through a second apparatus connector, comprising:

a first cable connector adapted to be coupled to said first apparatus connector;

a second cable connector adapted to be coupled to said second apparatus connector;

an electrical cable coupling said first cable connector to said second cable connector, said electrical cable including a plurality of conductors;

a translation circuitry for translating digital communications provided at said first apparatus connector in said first protocol into digital communications at said second apparatus connector in said second protocol, and for translating digital communications provided at said second apparatus connector in said second protocol into digital communications at said first apparatus connector in said first protocol, wherein said translation circuitry determines said first protocol and enables a first protocol driver appropriate to said determined first protocol in said translation circuitry.

48. (new) A cable assembly as recited in claim 47, wherein said translation circuitry includes a memory that stores a collection of protocol drivers, and said translation circuitry selects said first protocol driver from said collection of protocol drivers.

49. (new) A cable assembly as recited in claim 47, wherein said translation circuitry includes a memory, and said first protocol driver is loaded through said first cable connector into said memory.

50. (new) A protocol translator for plug-and-play compatibility, comprising:

a first group of terminals for receiving first digital communications in a first protocol;

a second group of terminals for receiving second digital communications in a second protocol; and

a translation circuitry provided between said first group of terminals and said second group of terminals, wherein said translation circuitry determines said first protocol received at said first group of terminals and enables a first protocol driver appropriate to said determined first protocol in said translation circuitry, such that said translation circuitry translates said first digital communications in said first protocol provided at said first group of terminals into translated first digital communications in said second protocol at said second group of terminals, and also translates said second digital communications in said second protocol provided at said second group of terminals into translated second digital communications in said first protocol at said first group of terminals.

51. (new) A protocol translator as recited in claim 50, further comprising a memory coupled to said translation circuitry, wherein said memory stores a collection of protocol drivers, and said translation circuitry selects said first protocol driver from said collection of protocol drivers.

52. (new) A protocol translator as recited in claim 50, further comprising a memory coupled to said translation circuitry, wherein said first protocol driver is loaded through said first group of terminals into said memory.

53. (new) A method for plug-and-play compatibility of a protocol translation circuitry, said method comprising:

determining a first communication protocol received at a first group of terminals of said protocol translation circuitry;

enabling a first protocol driver appropriate to said determined first protocol in said protocol translation circuitry;